IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Wagdi W. Abadeer, et al.	**Examiner:**	Unassigned
Serial No.:	To be assigned	**Art Unit:**	Unassigned
Filed:	Herewith	**Docket:**	BUR920000082US2 (13647A)
For:	A WAFER LEVEL SYSTEM FOR PRODUCING BURN-IN/SCREEN, AND RELIABILITY EVALUATIONS TO BE PERFORMED ON ALL CHIPS SIMULATNEOUSLY WITHOUT ANY WAFER CONTACTING	**Dated:**	March 16, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. U.S. Patent No. 5,945,834, issued August 31, 1999 to Nakata, et al.;
2. U.S. Patent No. 5,898,629, issued April 27, 1999 to Beffa, et al.;

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number: EV244124857US
Date of Deposit: March 16, 2004

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Alexandria, VA 22313-1450.

Dated: March 16, 2004

Leopold Presser

3. U.S. Patent No. 5,831,445 issued November 3, 1998 to Atkins, et al.;

4. U.S. Patent No. 5,661,408 issued August 26, 1997 to Kamieniecki, et al.

5. U.S. Patent No. 5,625,297 issued April 29, 1997 to Arnaudov, et al.;

6. U.S. Patent No. 5,600,257 issued February 4, 1997 to Leas, et al.;

7. U.S. Patent No. 5,578,930 issued November 26, 1996 to Sheen.;

8. U.S. Patent No. 5,570,032 issued October 29, 1996 to Atkins et al.;

9. U.S. Patent No. 5,552,704 issued September 3, 1996 to Mallory, et al.;

10. U.S. Patent No. 5,528,159 issued June 18, 1996 to Charlton, et al.;

11. U.S. Patent No. 5,519,193 issued May 21, 1996 to Freiermuth, et al.;

12. U.S. Patent No. 5,498,974 issued March 12, 1996 to Verkuil, et al.;

13. U.S. Patent No. 5,489,538 issued February 6, 1996 to Rostoker, et al.;

14. U.S. Patent No. 5,485,091 issued January 16, 1996 to Verkuil;

15. U.S. Patent No. 5,442,297 issued August 15, 1995 to Verkuil;

16. U.S. Patent No. 5,440,241 issued August 8, 1995 to King, et al.;

17. U.S. Patent No. 5,412,328 issued May 2, 1995 to Male, et al.;

18. U.S. Patent No. 5,424,651 issued June 13, 1995 to Green, et al.;

19. U.S. Patent No. 5,399,101 issued March 21, 1995 to Campbell, et al.;

20. U.S. Patent No. 5,429,520 issued July 4, 1995 to Morlion, et al.;

21. U.S. Patent No. 5,389,556 issued February 14, 1995 to Rostoker, et al.;

22. U.S. Patent No. 5,279,975 issued January 18, 1994 to Deveraux, et al.;

23. U.S. Patent No. 5,216,362 issued June 1, 1993 to Verkuil;

24. U.S. Patent No. 5,047,711 issued September 10, 1991 to Smith, et al.;

25. U.S. Patent No. 5,030,908 issued July 9, 1991 to Miyoshi, et al.;

26. U.S. Patent No. 4,812,756 issued March 14, 1989 to Curtis, et al.;

27. U.S. Patent No. 3,796,955 issued March 12, 1974 to Bhattacharyya, et al.;

28. "WAFER LEVEL TEST AND BURN IN", IBM Technical Disclosure Bulletin, January 1992, pp. 401 - 404;

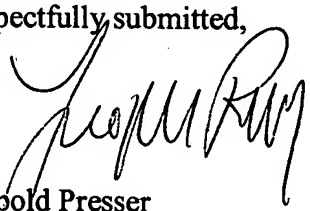
29. "MULTI-LAYER CERAMIC SPACE TRANSFORMER FOR WAFER LEVEL STRESS", IBM Technical Disclosure Bulletin, April 1991, pp. 385 - 386; and

30. "WAFER BURN-IN ISOLATION CIRCUIT", IBM Technical Disclosure Bulletin, November 1989, pp. 442 - 443.

Pursuant to 37 C.F.R. §1.98(d), copies of the above listed references are not provided, as these references were previously submitted to the Examiner in connection with parent case, U.S. Serial Number 09/811,915, filed March 19, 2001.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R §1.97(b), no statement or fee is required.

Respectfully submitted,



Leopold Presser
Registration No. 19,827
Attorney for Applicants

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343

LP:jy
Enclosure: PTO Form-1449

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE
(REV. 7-80)PATENT AND TRADEMARK OFFICE

LIST OF PRIOR ART CITED BY APPLICANT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
13647A (BUR20000082US2)	Unassigned
Applicant Wadgi W. Abadeer, et al.	
Filing Date Herewith	**Group** Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA	5,945,834	8/31/99	Nakata, et al.			
	AB	5,898,629	4/27/99	Beffa, et al.			
	AC	5,831,445	11/3/98	Atkins, et al.			
	AD	5,661,408	8/26/97	Kamieniecki, et al.			
	AE	5/625,297	4/29/97	Arnaudov, et al.			
	AF	5,600,257	2/4/97	Leas, et al.			
	AF	5,578,930	11/26/96	Sheen			
	AH	5,570,032	10/19/96	Atkins, et al.			
	AI	5,552,704	9/3/96	Mallory, et al			
	AJ	5,528,159	6/18/96	Charlton, et al.			
	AK	5,519,193	5/21/96	Freiermuth, et al.			
	AL	5,489,974	5/12/96	Verkuil, et al.			
	AM	5,489,538	2/6/96	Rostoker, et al.			
	AN	5,485,091	1/16/96	Verkuil			
	AO	5,442,297	8/15/95	Verkuil			
	AP	5,440,241	8/8/95	King, et al.			
	AQ	5,412,328	5/2/95	Male, et al.			
	AR	5,424,651	6/13/95	Green, et al.			
	AS	5,399,101	3/21/95	Campbell, et al.			
	AT	5,429,520	7/4/93	Morlion, et al.			

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		"WAFER LEVEL TEST AND BURN IN", IBM Technical Disclosure Bulletin, January 1992, pp. 401-404;
		"MULTI-LAYER CERAMIC SPACE TRANSFORMER FOR WAFER LEVEL STRESS", IBM Technical Disclosure Bulletin, April 1999, pp. 385 - 386;
		"WAFER BURN-IN ISOLATION CIRCUIT", IBM Technical Disclosure Bulletin, November 1989, pp. 442-443

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**